Thermal Limits for Integration of Directly Modulated Lasers with Driver IC on SOI

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Abstract: A study of thermal crosstalk between III-V hybrid integrated directly modulated laser diodes and driver IC in BiCMOS technology on SOI is presented. We derived design rules and cooling requirements from thermal modelling.

I. Introduction
The demand of high data rates in recent years has led to an increased interest in integrated photonics technologies, in particular in the new field of silicon photonics. A very promising application of silicon photonics is hybrid integration of directly modulated (DML) laser diodes with the driver IC. Advantages of this configuration are small form factor and low power consumption due to short RF connections. So far DMLs were limited to a bandwidth below 15 GHz. However recent advances in modulation bandwidth of InGaAsP Passive Feedback DFB Laser Diodes up to 40 GHz [1] make these devices very interesting for direct integration with driver IC. In combination with well established BiCMOS electronics highly efficient and low cost devices for data transmission are feasible. Due to the possibility of hybrid integration of both photonics and electronics on silicon on insulator (SOI) the advantages of both technologies can be exploited in one device. However, this approach introduces difficulties, especially in thermal management. In addition to the lack of power scaling in silicon photonics, which makes power densities increase even faster than in microelectronics, thermal crosstalk between photonic and electronic devices is expected. Because of comparatively high temperature sensitivity of photonic components the temperature distribution in such chips should be considered.

A study of thermal crosstalk of high bandwidth DML devices [1] and BiCMOS driver IC in an existing 0.25 µm SiGe BiCMOS technology was performed. As a starting point experimental results of integrated DFB laser diodes were used to calibrate a numerical model, which was utilized to derive design rules and cooling requirements for co-integration of DML devices and BiCMOS driver.

II. DFB Laser Integration on SOI – calibration of thermal model
In this study results of DFB laser diodes hybrid integrated on SOI by means of AuSn flip-chip soldering were used [2]. The thermal model was calibrated with a measurement of the wavelength shift vs. pump power for an AuSn flip-chip soldered DFB-laser. (i.e. determine thermal contact resistance).

The model used for our simulations comprised a simple flip-chip mounted DML on AuSn bumps and realistic thermal design power of a 40 GBit/s driver circuit in 0.25 µm BiCMOS technology. The whole setup can be seen in Fig. 1 (a). The power consumption of the laser was ~250 mW and the heat dissipation of the driver circuit added up to 0.95 W.

III. Self Heating Laser on SOI: For the first series of simulation the impact of SOI layer thicknesses tSi and tox of the silicon and oxide layers on the temperature distribution in a single externally driven laser was determined. As can be seen from Fig. 2 (a) the low
thermal conductivity of the oxide compared to that of silicon results in an increased temperature when $t_{ox}$ increases, while an increased $t_{Si}$ leads to a better capability of heat spreading in the silicon layer and hence to a lower temperature in the laser (Fig. 2 (b)).

![Figure 2](image-url)  
Figure 2: (a) Maximum temperature in the laser with varying $t_{ox}$ and constant $t_{Si}$ of 4 µm. (b) Maximum temperature with varying $t_{Si}$ and $t_{ox}$ of 1, 2 and 3µm. Ambient Temperature (heat sink) at 22°C. The higher temperature in graph (a) compared to Figure 1 (b) is due to higher power consumption of the high bandwidth DML.

Also one can observe that with a thin $t_{ox}$ the effect of heat spreading in the silicon layer vanishes and the temperature in the laser hardly changes as a function of $t_{Si}$.

**Laser on Backend:** The natural choice would be to integrate the DML directly on the passivation of the driver IC, which is required for the electronics wiring of the integrated circuit. However, when directly mounted on a low-k passivation of a driver IC (Fig. 3 (b)) the temperature rise in the laser becomes severe, which can be ascribed to a: the short distance between driver and laser and b: the extremely low thermal conductivities of the low-k materials. Fig. 3 (a) shows the influence of different low-k materials with a thickness of 10 µm on the temperature in the laser. With most thermal conductivities of low-k materials lying between 0.1 and 0.2 W/mK it is clear that this integration scheme is prohibitive for laser integration. As we will see in the next section spatial separation eases the problem of such high temperatures.

![Figure 3](image-url)  
Figure 3: Influence of low-k passivation materials on temperature in the laser when directly mounted on the operated driver.

**IV. Cross Heating**

**Single device:** When operating multiple devices on a single chip thermal crosstalk could lead to unwanted effects. Therefore the cross heating between multiple lasers and between laser and driver circuit has been simulated.

We measured the temperature rise in a laser at the active layer caused by another laser or the driver circuit. The simulations were performed with two different layer thicknesses

(I) $t_{ox} = 2 \mu m$, $t_{Si} = 0.2 \mu m$ and  
(II) $t_{ox} = 1 \mu m$, $t_{Si} = 1.5 \mu m$.

The results are shown in Fig. 4 as a function of the distance between the two lasers (a) and between laser and driver circuit (b). Since the overall heat generation of the driver circuit is much higher than that of the laser, the temperature rise in Fig. 4 (b) is also much higher.

![Figure 4](image-url)  
Figure 4: Temperature rise at active layer due to (a) another laser and (b) the driver circuit (distance edge to edge)

Although without large effect in our simulations, it is clear that the thickness of the silicon layer has the most impact on thermal crosstalk due to its high thermal conductivity.

**Laser-Driver Array:** Because of the linearity of the heat equation one can simply superpose temperature fields of different sources. Fig. 5 shows the temperature elevation in the active layer in a 4 laser array caused by cross heating as a
function of the distance between lasers.

![Figure 5: Temperature rise at the active layer caused by 3 other lasers and 4 driver circuits with a very dense lateral spacing between lasers (edge to edge) and corresponding driver.](image)

V. Non ideal heat sink – Design Rules for a >100 GBit/s CWDM transceiver

So far an ideal heat sink was assumed. If the amount of heat generated on a chip raises above a certain density, the nature of the heat sink starts to have a major influence on the temperature distribution. For this reason a design optimization for a 4 channel CWDM transceiver for bit rates above 100 Gbit/s was conducted with respect to the cooling mechanism, characterized by the heat transfer coefficient $h$. The overall heat generated by the four lasers and their driver circuits amounted to 4.8 W. An upper boundary for heating was derived from an CWDM AWG filter curve (Fig. 6). To avoid inter-channel crosstalk and unwanted attenuation a 1.2 nm maximum deviation (10 % of the FWHM from the peak), which translates to a temperature rise of 12 °C in a laser, was set.

The value of the heat transfer coefficient $h$ was set according to three types of cooling: forced air convection, peltier cooling and forced water convection. As a result the required spacing of components on the chip was retrieved. In order to stay inside the 12 °C tolerance through cross heating the distances depicted in Table 1 between lasers $d_{ll}$ and between laser and driver circuit $d_{ld}$ should be observed.

As can be seen, it is impossible to stay within the 10 % tolerance on a 1x1 cm chip using forced air convection. In contrast, when cooling the setup with water, one would have no problem at all handling the heat generation, regardless of spacing parameters. The most popular cooling mechanism for photonic devices - the peltier element – demands special attention to power densities. Spacing the thermally active devices according to Table 1 should ensure a durable operation within the temperature tolerance.

VI. Conclusions

The results of a thermal simulation of integrated lasers on SOI were presented. Our simulations showed the following requirements for direct integration of laser diodes and driver IC: Spatial separation, peltier cooling or better and minimum spacing between thermally active devices of the order of 0.5 mm. It has become clear that mounting on top of low-k material is the most problematic design from thermal perspective. However spatial separation of driver circuit and laser and mounting of the laser on silicon will circumvent excessive temperatures, even with non ideal heat sinks like peltier coolers. Our simulations show that SOI is a promising substrate for monolithical high density integration of lasers and electronics.

References